EL465782038

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/388,857
Priority Filing Date ..... September 1, 1999
Inventor ..... Luan C. Tran
Assignee ..... Micron Technology, Inc.
Priority Group Art Unit 1765
Priority Examiner ..... L. Schillinger
Attorney's Docket No. MI22-1637
Title: Semiconductor Processing Methods Of Forming Transistors, Semiconductor Processing Methods Of Forming Dynamic Random Access Memory Circuitry, And Related Integrated Circuitry

PRELIMINARY AMENDMENT

To: Assistant Commissioner for Patents
Washington, D.C. 20231

From: Frederick M. Fliegel, Ph.D.
Tel. 509-624-4276; Fax 509-838-3424
Wells, St. John, Roberts, Gregory & Matkin P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3817

Sir:

This is a preliminary amendment accompanying a Request for Divisional Application for the above-entitled patent application. Prior to examining the application, please enter the following amendments.

AMENDMENTS

In the Specification

On page 1, after the title insert:

CROSS REFERENCE TO RELATED APPLICATION

This patent application is a Divisional Application of U.S. Patent Application Serial No. 09/388,857, filed September 1, 1999, entitled "Semiconductor Processing Methods Of Forming Transistors, Semiconductor Processing Methods Of Forming Dynamic Random Access Memory Circuitry, And Related Integrated Circuitry", naming Luan C. Tran as inventor, the disclosure of which is incorporated by reference.

Replace the paragraph beginning on page 10, line 21, and extending through p. 11, line 9 with the following:

Also shown in Fig. 7 is a sense amplifier circuit 50 including cross-coupled transistors 52 and 54. In one embodiment, the transistors 52 and 54 are formed to have a low threshold voltage V_{tl}. When the signal CSAL goes to logic "1", the common node labeled RNL* equilibrates the potentials on sources of the transistors 52 and 54 in preparation for reading stored data from memory cells in a memory array (not shown). In the example shown in Fig. 7, the circuit 40 acts as a pull-down circuit and equilibrates the node RNL* to ground. Use of multiple transistors 42, 44 and 46 having different threshold voltages facilitates ("softens") sensing at the beginning of the sensing cycle and also facilitates more rapid sensing at the end of the cycle when differential signals have been developed by the transistors 52 and 54.

In the Drawings

Please modify Fig. 3 as shown in the enclosed marked-up-in-red copy thereof. Substitute formal drawings are also enclosed, including a corrected Fig. 3.

In the Claims

Please cancel claims 1-7 without prejudice.

REMARKS

This application is a divisional application of U.S. Patent Application Serial No. 09/388,857, and is being filed responsive to a restriction requirement therein. Accordingly, claims 1-7 have been canceled without prejudice. Claims 8-50 remain in the application for consideration.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made**."

This application is believed to be in condition for allowance and action to that end is requested. The Examiner is requested to telephone the undersigned in the event that the next office action is one other than a Notice of Allowance. The undersigned is available during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: April 12, 2001 By: _____

Frederick M. Fliegel, Ph.D.
Reg. No. 36,138

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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37 CFR § 1.121(b)(1)(iii) AND 37 CFR § 1.121(c)(1)(ii) FILING REQUIREMENTS TO ACCOMPANY PRELIMINARY AMENDMENT

Deletions are bracketed, additions are underlined.

In the Specification

On page 1, after the title, insert:

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This patent application is a Divisional Application of U.S. Patent Application Serial No. 09/388,857, filed September 1, 1999, entitled "Semiconductor Processing Methods Of Forming Transistors, Semiconductor Processing Methods Of Forming Dynamic Random Access Memory Circuitry, And Related Integrated Circuitry", naming Luan C. Tran as inventor, the disclosure of which is incorporated by reference.

The paragraph beginning on page 10, line 21, and extending through p. 11, line 9 has been amended as follows:

Also shown in Fig. 7 is a sense amplifier circuit 50 including cross-coupled transistors 52 and 54. In one embodiment, the transistors 52 and 54 are formed to have a low threshold voltage V_{tl}. When the signal CSAL goes to logic "1", the common node labeled RNL* equilibrates the potentials on sources of the transistors 52 and 54 in preparation for reading stored data from memory cells in a memory array (not shown). In the example shown in Fig. 7, the circuit 40 acts as a pull-down circuit and equilibrates the node RNL* to ground. Use of multiple transistors 42, 44 and 46 having different threshold voltages facilitates ("softens") sensing at the beginning of the sensing cycle and also facilitates more rapid sensing at the end of the cycle when differential signals have been developed by the transistors 52 and 54.

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Fig. 3 has been modified as shown in the enclosed marked-up-in-red copy thereof. Substitute formal drawings are also enclosed, including a corrected Fig. 3.

In the Claims

Claims 1-7 have been canceled without prejudice.

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Assistant Commissioner for Patents
Washington, D. C. 20231
Attention: Official Draftsman

SUBSTITUTE DRAWING REQUEST

Enclosed is a Red-line drawing of Fig. 3 along with a corrected formal drawing, and substitute formal drawings, Figs. 1-7. Please enter the enclosed substitute formal drawings in the above-referenced application in place of drawings originally filed. The content of the drawings are identical to those now on file in this application.

Acknowledgment of receipt of the formal drawings and their acceptance into the file is requested.

Respectfully submitted,

Date: April 12, 2001

By: _____

Frederick M. Fliegel, Ph.D.
Reg. No.: 36,138
WELLS, ST. JOHN, ROBERTS,
GREGORY & MATKIN P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828
(509) 624-4276

Enclosures: 1 Red-line Drawing, Fig. 3 & 2 Sheets of Formal Drawings, Figs. 1-7.

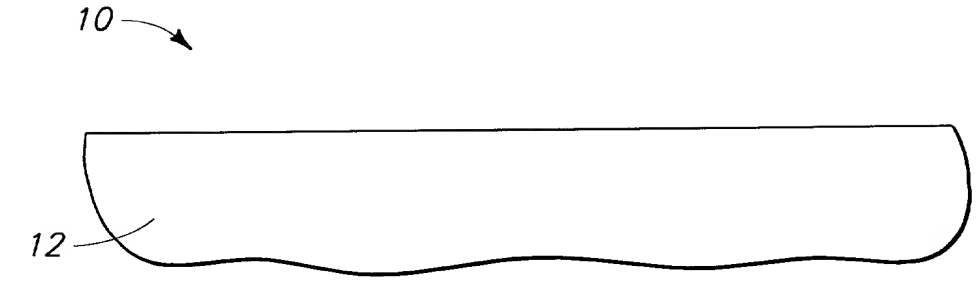

Fig 1

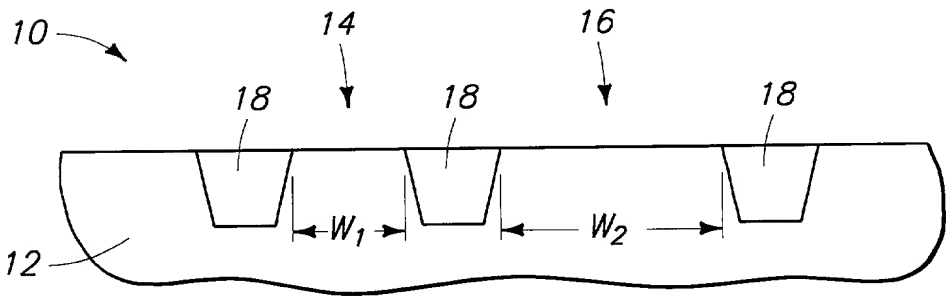

Fig 2

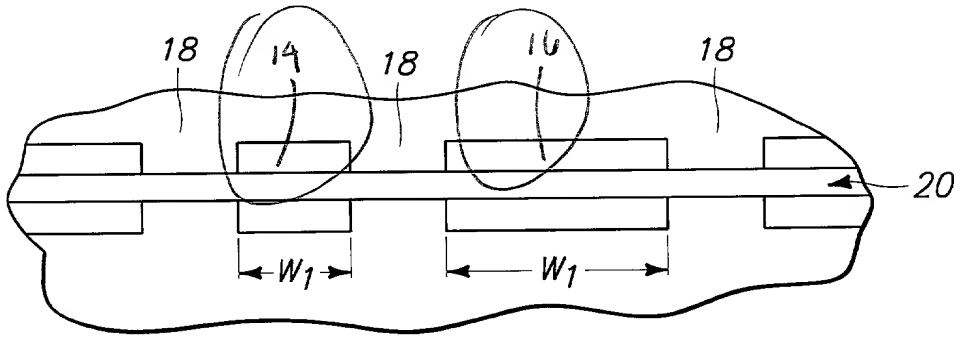

Fig 3

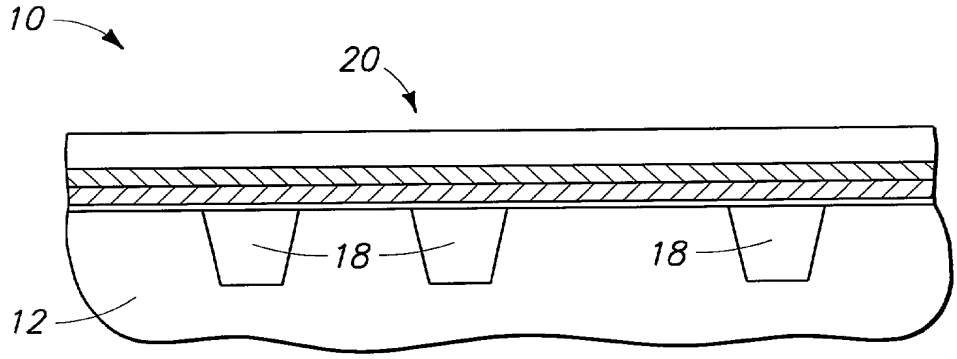

Fig 4

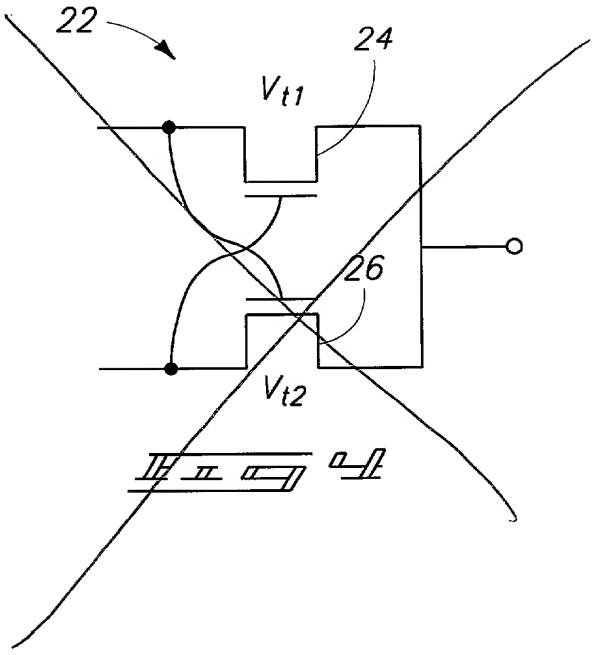

Fig 4

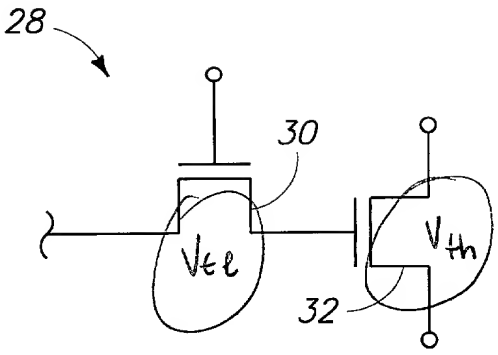

Fig 5

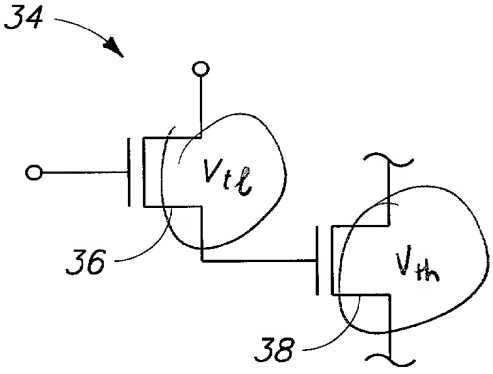

Fig 6

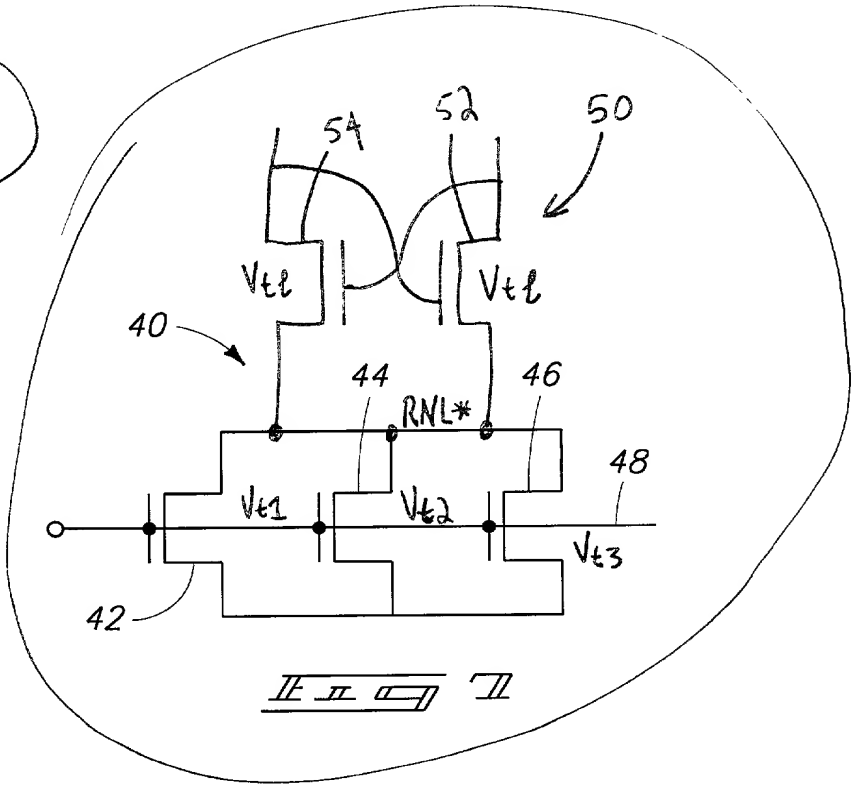

Fig 7

Approved for Public Release

Fig 1

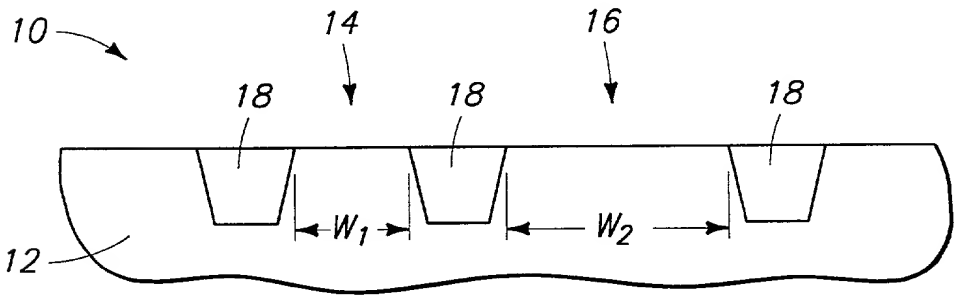

Fig 2

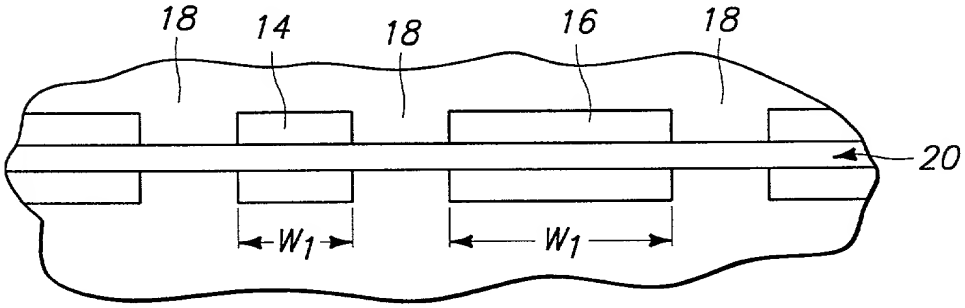

Fig 3

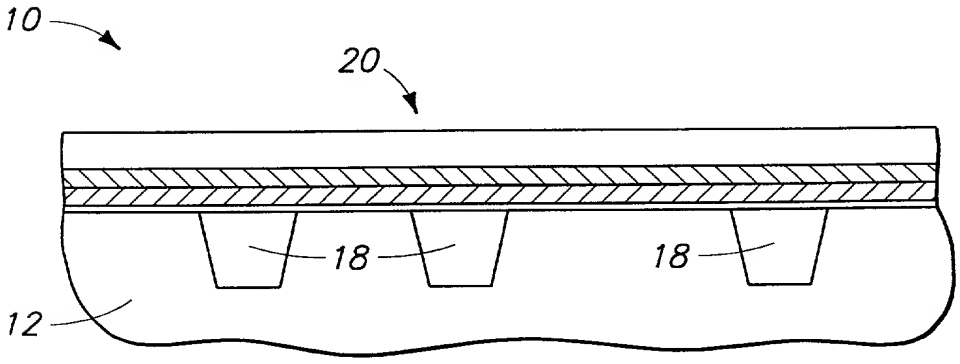

Fig 4

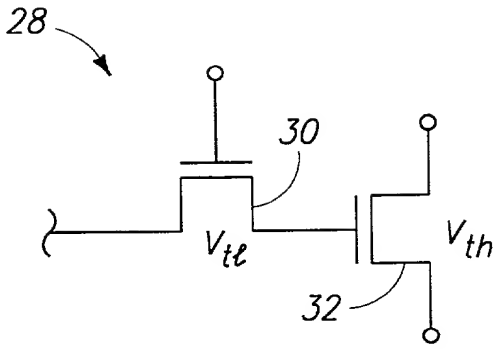

Fig 5

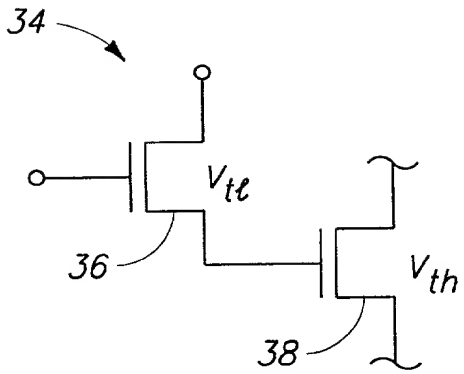

Fig 6

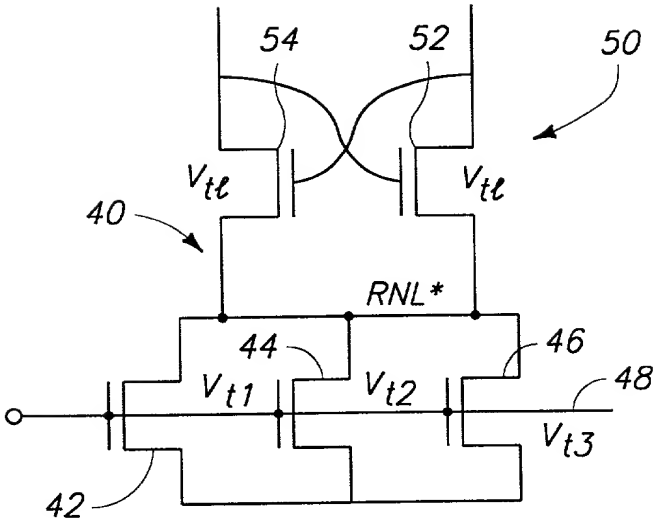

Fig 7